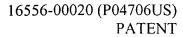IN THE SPECIFICATION

Please amend the following paragraph of the specification which is located at page 6, line 5 to page 7, line 3 as follows:

Depending upon functions to be performed by class processor 10, one or more localized read/write memories 14, 16, ~~and 18~~ and 20 are provided and interconnected with special purpose processor 12 so as to be directly accessible to it, i.e., visible and addressable in its memory space. Memory 14 is a private localized read/write memory 14 that is used by and is accessible only by special purpose processor 12 through its implemented methods. Memory 16 is a localized protected read/write memory that is used by special purpose processor 12 to store and/or read data accessible only by other class processors 10 of the same grouping or class. For example, where class processor 10 is a fast Fourier transform (FFT) processor, another class processor 10 (not shown in Figure 1) that implements a similar function or functions is able to access protected memory 16. Examples of two class processors sharing protected localized read/write memory 16 are two FFT processors used at the same time, or an FFT processor and a discrete Fourier transform (DFT) processor that computes discrete Fourier transforms somewhat differently, for example, using a Winograd DFT. Access to protected localized read/write memory 16 is provided by one or both of a direct interconnection 18 from protected localized read/write memory 16 to the other class processor 10 or by providing special purpose processors 12 of each class processor 10 belonging to the same class with special knowledge of messages that can be passed between class processors 10 of that class. Memory 20 is a public read/write memory that can be addressed by other components, including a host processor (not shown in Figure 1). In one embodiment, public read/write memory is directly accessible via a memory mapped mailbox or an application program interface (API) module 22. It will be recognized by those skilled in the art that not all embodiments of class processors 10 require all three types of memories 14, 16, and 20. API module 22 comprises a communication port, for example, a

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hardware or software communication port that including a memory-mapped dual port memory bank. In another embodiment, API module 22 includes a memory stack.